H2P1: Voltage-Divider Design

The resistances of commercially-available discrete resistors are restricted to particular sets. For example, the available values of resistors with 10\% tolerance are selections from the $E_{12}$ set multiplied by a power of ten from $10^0$ through $10^5$. The $E_{12}$ set is:

$$E_{12} = \{10, 12, 15, 18, 22, 27, 33, 39, 47, 56, 68, 82\}$$

Thus, you can buy 10\% resistors with a nominal resistance of 330\,\Omega or 33\,k\,\Omega, but not 350\,\Omega. Furthermore, the "tolerance" means that if you buy a 10\% 390\,\Omega resistor you can be sure that its resistance is between 351\,\Omega and 429\,\Omega.

In this problem we need to choose 10\% resistors to make a voltage divider that meets a given specification.

We are given an input voltage $V_in=60.0\,V$, and we need to provide an open-circuit output voltage of $V_{out} \approx 24.0\,V$. An additional requirement is that the Thevenin resistance as seen from the output terminals is between $10k\,\Omega$ and $30k\,\Omega$. Assume first that the resistors have their nominal resistance. Come up with resistors $R_1$ and $R_2$ such that the divider ratio $V_{out}/V_{in}$ is within 10\% of the requirement.

Of course, the resistances you chose are just nominal. Given that they are only guaranteed to have resistances within 10\% of the nominal value, what is the largest and smallest value that $V_{out}$ may have?

Enter your values below.

R1 (in Ohms):

unanswered
R2 (in Ohms):

unanswered

Vmax (in Volts):

unanswered

Vmin (in Volts):

unanswered

Explanation:

For this solution, we assume that \( V_{in}=30\, V, V_{out}=7.5\, V, 10\, k\Omega \leq R_{TH} \leq 30\, k\Omega \).

We apply the voltage divider equation:

\[
V_{out} = V_{in} \frac{R_2}{R_1 + R_2} \rightarrow 7.5 = 30 \frac{R_2}{R_1 + R_2} \Rightarrow 30R_2 = R_1 + R_2, \text{ or } 3R_2 = R_1
\]

Since we know that the chosen resistors must obey the ratio 3:1, we choose resistances from the list of nominal resistances. Choosing \( R_1 = 56\, k\Omega \) and \( R_2 = 18\, k\Omega \), we approximately observe this resistor ratio.

To verify that the equivalent thevenin resistance is within the required limit, we simply calculate the equivalent resistance of these two resistors as if they were in parallel, which is given by

\[
R_{TH} = R_1 R_2 / (R_1 + R_2) = 13.62\, k\Omega
\]

Finally, to calculate the maximum and minimum voltages, we apply the following formula:

\[
V_{max} = V_{in} \times (1.1)(R_2)(0.9)(R_1) + (1.1)(R_2) = 8.461\, V
\]

\[
V_{min} = V_{in} \times (0.9)(R_2)(1.1)(R_1) + (0.9)(R_2) = 6.246\, V
\]

- **H2P2: Solar Power**

A simple model of a photovoltaic solar cell is a current source, with the current proportional to the amount of sunlight falling on it. A more accurate model includes a diode (a nonlinear
element we will see later). There is some leakage current that we can model with a parallel resistor, and there is a voltage drop in the interconnect that we can model with series resistances connecting to the load resistor. So a crude model of a complete system might be the circuit shown below.

In this system we have $I=0.1\,\text{A}$, $R_p=6.0\,\Omega$, and $R_s=1.3\,\Omega$.

You are to determine the load resistance, $R_L$, for which the maximum power is transferred to the load. (Hint: remember your calculus!)

What is this optimum load resistance (in Ohms)?

unanswered

8.6

What is the power (in Watts) that is delivered to this best load resistance?

unanswered

0.01047

What is the Thevenin equivalent resistance (in Ohms) of the power source as seen by the load resistance?

unanswered

8.6
Hmnmnmnm.

Explanation:

The optimum load resistance occurs when the maximum power is transferred. To find that point, we take the derivative of an expression for power with respect to the load resistance.

But first, we can convert the Norton sub-circuit on the left side of the circuit diagram to its Thevenin equivalent, which gives us a voltage \( V_{R_p} = (0.1)(6.0) = 0.6 \) Volts. The \( R_{TH_{new}} \) of the entire new circuit will be: \( R_s + R_p + R_s + R_L \). The equation for power consumed by the load is \( P = I^2 R_L \), where:

\[
I = V_{R_{TH_{new}}} = 0.6R_s + R_p + R_s + R_L
\]

Setting the derivative of the expression for power equal to zero and solving for the load resistance will give us the optimal load resistance for maximum power transfer.

\[
dP/dR_L = d([0.6R_s + R_p + R_s + R_L]2 \times R_L) dR_L = 0
\]

Simplifying the power expression by substituting known variables and re-naming \( R_L \) as \( x \):

\[
= 0.36(\frac{d}{dx}[x(8.6 + x)^2]) = 0
\]

Applying product rule:

\[
= 0.36(x(\frac{d}{dx}[1(x+8.6)^2]) + \frac{d}{dx}(x)(x+8.6)^2)
\]

\[
= 0.36(x[-2(x+8.6)^3] + 1(x+8.6)^2)
\]

Equating the expression to zero, we solve for \( x \):

\[
0 = -2x(x+8.6)^3 + 1(x+8.6)^2
\]

\[
\therefore x = R_L = 8.6\Omega
\]

To solve for power consumed, we simply use the following expression:

\[
P = I^2 R_L \rightarrow I = 0.6 \text{V} \sqrt{17.2\Omega} \text{ and } R_L = 8.6\Omega
\]

\[
\therefore P = 0.01047 \text{ W}
\]

\( R_{TH} \) seen by the load resistance is: \( R_s + R_p + R_s = 8.6\Omega \)

Note that the optimum load resistance is the same as the thevenin equivalent resistance.
In the figure above Circuit 1 is a two-input single-output logic circuit. The truth table for a two-input function has four rows as shown below:

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>w</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>x</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>y</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>z</td>
</tr>
</tbody>
</table>

Fill in the values of F in the truth table for Circuit 1.

What is the entry in the box labeled \( w \)?

unanswered

1

What is the entry in the box labeled \( x \)?

unanswered

0
What is the entry in the box labeled $y$?

unanswered

0

What is the entry in the box labeled $z$?

unanswered

1

The figure below shows three additional two-input single-output logic circuits. Two of these circuits are equivalent to Circuit 1, i.e., they compute the same logic function.

Circuit 2

Circuit 3
Which of these circuits is **not** equivalent to Circuit 1? (Enter the number of the circuit)

unanswered

4

Explanation:

Circuit 1 displays a circuit which evaluates the boolean expression \((A^\bar{\text{\backslash}} + B) \cdot (A + B^\bar{\text{\backslash}})\) which provides the following truth table:

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
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<td>1</td>
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<td>1</td>
</tr>
</tbody>
</table>

As a sidenote, this particular truth table is associated with the operation XNOR, and which looks like ![XNOR gate](image) when drawn as a logic gate.

Circuit 2 evaluates \((A^\bar{\text{\backslash}} \cdot B^\bar{\text{\backslash}}) + (A \cdot B)\) and Circuit 3 evaluates \((A + B^\bar{\text{\backslash}}) + (A \cdot B)\), which both simplify to XNOR and give the same truth table as Circuit 1.

Circuit 4, on the other hand, implements \((A^\bar{\text{\backslash}} \cdot B) + (A \cdot B^\bar{\text{\backslash}})\) which gives the truth table for XOR, shown below.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>0</td>
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</tr>
</tbody>
</table>

If you were wondering, the gate for XOR looks like ![XOR gate](image).