Crystal Growth and Wafer Fabrication

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VIT
• Crystal growth
  – Obtaining sand
  – Raw Polysilicon
  – Czochralski Process (growing single crystal ingots)
  – Ingot size and Characterization

• Wafer Fabrication
  – Slicing Ingots
  – Primary and Secondary Flats (Orientation)
  – Wafer Lapping
  – Wafer Etching
  – Wafer Polishing
  – Wafer Cleaning
Basic Process Steps for Wafer Preparation

- Crystal Growth
- Shaping
- Wafer Slicing
- Wafer Lapping and Edge Grind
- Etching
- Polishing
- Cleaning
- Inspection
- Packaging
Obtaining the Sand

• The sand used to grow the wafers has to be a very clean and good form of silicon.

• For this reason not just any sand scraped off the beach will do.

• Most of the sand used for these processes is shipped from the beaches of Australia.
Preparation of MGS from Quartz Sand

- Put pure quartz sand and carbon into high-temperature furnace.
- Carbon can be in form of coal, coke or even piece of wood.
- At high temperature, carbon starts react with silicon dioxide to form carbon oxide.
- This process generates polycrystalline silicon with about 98% to 99% purity called crude or Metallurgical-grade silicon.
- The chemical reaction as follows
  \[ \text{SiO}_2 + 2\text{C} \rightarrow \text{Si} + 2\text{CO} \]
Silicon Purification

- Crude silicon is ground into fine powder.
- Then silicon powder is introduced into reactor to react with HCl(vapor), forming (TCS, SiHCl₂) vapor at about 300°C.

The chemical reaction as follows

\[ \text{Si} + 3\text{HCl} \rightarrow \text{SiHCl}_3 + \text{H}_2 \]

TCS vapor then goes through series of filters, condensers, and purifiers to get ultra high-purity liquid TCS, with purity higher than 99.999999999%. 
Preparation of EGS form TCS

• High purity TCS is one of the most commonly used silicon source precursors for silicon deposition.
• At high temperature, TCS can react with hydrogen and deposit high purity polysilicon.
• The reaction as follows
• $\text{SiHCl}_3 + \text{H}_2 \rightarrow \text{Si} + 3\text{HCl}$
• The high purity polysilicon crystalline silicon is called electron grade silicon or EGS.
Raw Polysilicon

• Raw polycrystalline silicon produced by mixing refined trichlorosilane with hydrogen gas in a reaction furnace.

• The poly-crystalline silicon is allowed to grow on the surface of electrically heated tantalum hollow metal wicks.
Polysilicon Ingots

• The polycrystalline silicon tubes refined by dissolving in hydrofluoric acid producing polysilicon ingots.

• Polycrystalline silicon has randomly oriented crystallites, electrical characteristics not ready for device fabrication.

• Must be transformed into single crystal silicon using crystal pulling
Czochralski (CZ) crystal growing

Step: 1 Preparation of high purity molten silicon
Step: 2 Dipping Seed crystal
Step: 3 Pulling the seed upwards
Czochralski (CZ) crystal growing

- All Si wafers come from "Czochralski" grown crystals. Polysilicon is melted, then held just below 1417 °C, and a single crystal seed starts the growth. Pull rate, melt temperature, and rotation rate control the growth.

- It contains < 1 ppb impurities. Pulled crystals contain O (~10^{18} \text{ cm}^{-3}) and C (~10^{16} \text{ cm}^{-3}), plus dopants placed in the melt.
Silicon Ingot Grown by CZ Method

Photograph courtesy of Kayex Corp., 300 mm Si ingot

Photo 4.1
Examples of completed ingots
Ingot Sizes

- Most ingots produced today are 150mm (6") and 200mm (8") diameter,
- For the most current technology 300mm (12") and 400mm (16") diameter ingots are being developed.
Ingots are characterized by the orientation of their silicon crystals. Before the ingot is cut into wafers, one or two "flats" are ground into the diameter of the ingot to mark this orientation.
• Crystal growth
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  – Slicing Ingots
  – Primary and Secondary Flats (Orientation)
  – Wafer Lapping
  – Wafer Etching
  – Wafer Polishing
  – Wafer Cleaning
Slicing Ingots

- The ingot is ground into the correct diameter for the wafers.
- Then it is sliced into very thin wafers.
- This is usually done with a diamond saw.
Some wafers in storage trays
Lattice Orientation

• The lattice orientation refers to the organized pattern of the silicon crystals in the wafer and their orientation to the surface.

• The orientation is obtained based on the orientation of the crystal that is placed into the molten silicon bath.

• The different orientations have different benefits and are used in different types of chips.
<100> Lattice Orientation

- This lattice orientation is used for MOS (metal oxide semiconductor), Bi-CMOS, & GaAs types of chips.
<111> Lattice Orientation

- This orientation is used for Bipolar types of chips
Different flats for orientation

**Wafer Flats** - orientation for automatic equipment and indicate type and orientation of crystal.

**Primary flat** - The flat of longest length located in the circumference of the wafer. The primary flat has a specific crystal orientation relative to the wafer surface; major flat.

**Secondary flat** - Indicates the crystal orientation and doping of the wafer.
Wafer Lapping

- The sliced wafers are mechanically lapped using a counter-rotating lapping machine and aluminum oxide slurry. This flattens the wafer surfaces, makes them parallel and reduces mechanical defects like saw markings.
Wafer Lapping Machine
Wafer Etching

• After lapping, wafers are etched in a solution of nitric acid/ acetic acid or sodium hydroxide to remove microscopic cracks or surface damage created by the lapping process.

• The acid or caustic solution is removed by a series of high-purity RO/DI water baths
Wafer polishing

Next, the wafers are polished in a series of combination chemical and mechanical polish processes called CMP.

The wafers are held in a hard ceramic chuck using either wax bond or vacuum and buffed with a slurry of silica powder, RO/DI water and sodium hydroxide.
Wafer Cleaning

A. Solvent Removal
1. Immerse in boiling trichloroethylene (TCE) for 3 min.
2. Immerse in boiling acetone for 3 min.
3. Immerse in boiling methyl alcohol for 3 min.
4. Wash in DI water for 3 min.

B. Removal of Residual Organic/Ionic Contamination
1. Immerse in a (5:1:1) solution of H$_2$O-NH$_4$OH-H$_2$O$_2$; heat solution to 75-80 °C and hold for 10 min
2. Quench the solution under running DI water for 1 min
3. Wash in DI Water for 5 min.

C. Hydrous Oxide Removal
1. Immerse in a (1:50) solution of HF-H$_2$O for 15 sec
2. Wash in running DI water with agitation for 30 seconds.

D. Heavy metal clean
1. Immerse in a (6:1:1) solution of H$_2$O-HCL-H$_2$O$_2$ for 10 min at a temperature of 75-80 °C
2. Quench the solution under running DI water for 1 min.
3. Wash in running DI water for 20 min.
Wafer Dimensions & Attributes

<table>
<thead>
<tr>
<th>Diameter (mm)</th>
<th>Thickness (μm)</th>
<th>Area (cm²)</th>
<th>Weight (grams/lbs)</th>
<th>Weight/25 Wafers (lbs)</th>
</tr>
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<tbody>
<tr>
<td>150</td>
<td>675 ± 20</td>
<td>176.71</td>
<td>28 / 0.06</td>
<td>1.5</td>
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<tr>
<td>200</td>
<td>725 ± 20</td>
<td>314.16</td>
<td>53.08 / 0.12</td>
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<tr>
<td>300</td>
<td>775 ± 20</td>
<td>706.86</td>
<td>127.64 / 0.28</td>
<td>7</td>
</tr>
<tr>
<td>400</td>
<td>825 ± 20</td>
<td>1256.64</td>
<td>241.56 / 0.53</td>
<td>13</td>
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</tbody>
</table>

Table 4.3
Increase in Number of Chips on Larger Wafer Diameters (Assume large 1.5 x 1.5 cm microprocessors)

Figure 4.13
## Developmental Specifications for 300-mm Wafer Dimensions and Orientation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Units</th>
<th>Nominal</th>
<th>Some Typical Tolerances</th>
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<tbody>
<tr>
<td>Diameter</td>
<td>mm</td>
<td>300.00</td>
<td>± 0.20</td>
</tr>
<tr>
<td>Thickness (center point)</td>
<td>μm</td>
<td>775</td>
<td>± 25</td>
</tr>
<tr>
<td>Warp (max)</td>
<td>μm</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Nine-Point Thickness Variation (max)</td>
<td>μm</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Notch Depth</td>
<td>mm</td>
<td>1.00</td>
<td>+ 0.25, -0.00</td>
</tr>
<tr>
<td>Notch Angle</td>
<td>Degree</td>
<td>90</td>
<td>+5, -1</td>
</tr>
<tr>
<td>Back Surface Finish</td>
<td></td>
<td></td>
<td>Bright Etched/Polished</td>
</tr>
<tr>
<td>Edge Profile Surface Finish</td>
<td></td>
<td></td>
<td>Polished</td>
</tr>
<tr>
<td>FQA (Fixed Quality Area – radius permitted on the wafer surface)</td>
<td>mm</td>
<td>147</td>
<td></td>
</tr>
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</table>


Table 4.4
Quality Measures

- Physical dimensions
- Flatness
- Microroughness
- Oxygen content
- Crystal defects
- Particles
- Bulk resistivity