4-Bit Fast Adder Design: Topology and Layout with Self-Resetting Logic for Low Power VLSI Circuits

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Abstract— **Dynamic logic families offer good performance over traditional CMOS logic. This is due to the comparatively high noise margins coupled with the ease of implementation. The main drawbacks of dynamic logic circuits are lack of design automation, charge sharing, feedthrough, charge leakage, single-event upsets, etc. But these draw backs can be eliminated using domino and NORA circuits but still lacks in the application of clock distribution grid and routing to dynamic gates that presents a problem to CAD tools and introduces issues of delay and skew into the circuit design process. A special dynamic logic circuit which resolves these issues is called Self-Resetting Logic (SRL). A new family of self-resetting logic (SRL) primitive gates and adder cells are presented in this paper which can eliminate the above cited issues. The operation of primitive and adder circuit are elucidated and it is simulated using microwind and LT-SPICE simulator. The analysis of basic gates and adder are compared with conventional dynamic logic circuit in terms of area, power dissipation and propagation delays at 0.12-µm 6metal layer CMOS technology is carried out.**

Keywords- **High speed, VLSI, Self-resetting logic (SRL), topologies, power dissipation**

I. INTRODUCTION

Dynamic logic circuits are widely used in modern low power VLSI circuits. These dynamic circuits are becoming increasingly popular because of the speed advantage over static CMOS logic circuits; hence they are widely used today in high performance and low power circuits. Normally in the design of flip-flops and registers, the clock distribution grid and routing to dynamic gates presents a problem to CAD tools and introduces issues of delay and skew into the circuit design process [1]. There are situations that permit the use of circuits that can be automatically precharge themselves (i.e., reset themselves) after a prescribed delays. These circuits are called postcharge or self-resetting logic which are widely used in memory decoders. A fundamental difficulty with dynamic circuits is the monotonicity requirement. In the design of dynamic logic circuits numerous difficulties may arise like charge sharing, feedthrough, charge leakage, single-event upsets, etc. In this paper novel energy-efficient self-resetting primitive gates followed by the design of adder logic circuits are proposed.

Addition is a fundamental arithmetic operation that is generally used in many VLSI systems, such as application-specific digital signal processing (DSP) architectures and microprocessors [2]. This module is the core of many arithmetic operations such as addition/subtraction, multiplication, division and address generation. Such high performance devices need low power and area efficient adder circuits. So this paper presents a design construction for primitive gates and adder circuits which reduce delay and clock skew when compared to the dynamic logic adder implementation. The operation of primitive and adder circuits are elucidated and it is simulated using microwind and LT-SPICE simulator and it is compared with dynamic logic circuit in terms of area, power dissipation and propagation delays at 0.12µm technology is carried out.

The remainder of this paper is organized as follows. Section II explains the limitation of dynamic circuits. Section III introduces the general concepts on SRL. Section IV describes the design of primitive gates, full adder, 4-bit parallel adder and carry look ahead adder. Section V presents the simulation results implemented in 0.12-µm CMOS technology. Section VI discusses a comparison and summary with dynamic logic implementation of the same design presented in SRL. The final section presents the conclusion.

II. LIMITATIONS OF DYNAMIC CIRCUITS

In today‘s fast processing environment, the use of dynamic circuits is becoming increasingly popular [5]. Dynamic CMOS circuits are defined as those circuits which have an additional clock signal inputs along with the default combinational circuit inputs of the static systems. Dynamic systems are faster and efficient than the static systems. MOS does not require the capacitances to be connected externally; thereby CMOS

dynamic systems are very advantageous. However, they suffer from some major drawbacks. They are:
1. Charge Leakage
2. Charge sharing
3. Clock Skew

The main problem is the potential for logic upset due to charge loss on a capacitor, and that is not acceptable to most designers. Charge may be lost via charge sharing, noise injection due to capacitive coupling, charge leakage, or α - particle hits. Once lost, it cannot be recovered and the circuit ceases to function correctly[3]. Dynamic circuits suffer from charge sharing problem because of parasitic capacitances at different nodes of a circuit. This results in lower voltage levels at the output terminals. In such circuit designs redistribution of charges takes place leading to charge sharing problems. It is common to use several stages of dynamic circuits to realize a Boolean function. Although same clock is applied to all these stages, it suffers from delay due to resistance and parasitic capacitances associated with the wire that carry the clock pulse. This delay is approximately proportional to the square of the length of the wire [4]. As a result, different amount of delays are experienced at different points in the circuit and the signal state changes that are supposed to occur in coincidence may never actually occur at the same time[9].

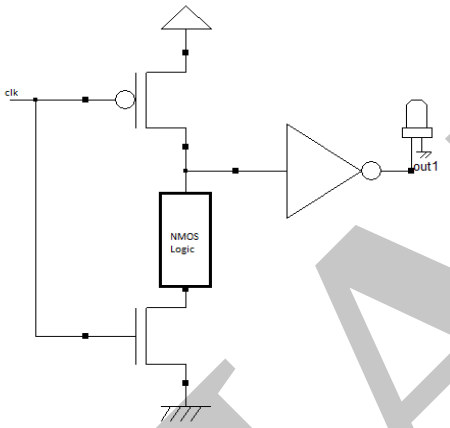


Fig. 1 Basic Topology of Dynamic Logic Circuit

The general topology of dynamic circuit is depicted in the Fig. 1. The circuit operation is defined in two modes. They are precharge and evaluation mode. During the precharge phase (when clk=0), the output node of the dynamic CMOS stage is precharged to a high logic level, and the output of the CMOS inverter (buffer) becomes low. When the clock signal rises at the beginning of the evaluation phase, there are two possibilies: the output node of the dynamic CMOS stage is either discharged to a low level through the NMOS circuitry (1 to 0), or it remains high. Consequently, the inverter output voltage can also make at most one transition during the evaluation phase, from 0 to 1. Regardless of the input voltages applied to the dynamic CMOS stage, it is possible for the buffer output to make a 1 to 0 transition during the evaluation phase. Fig. 2 shows the primitive gates using dynamic circuit.

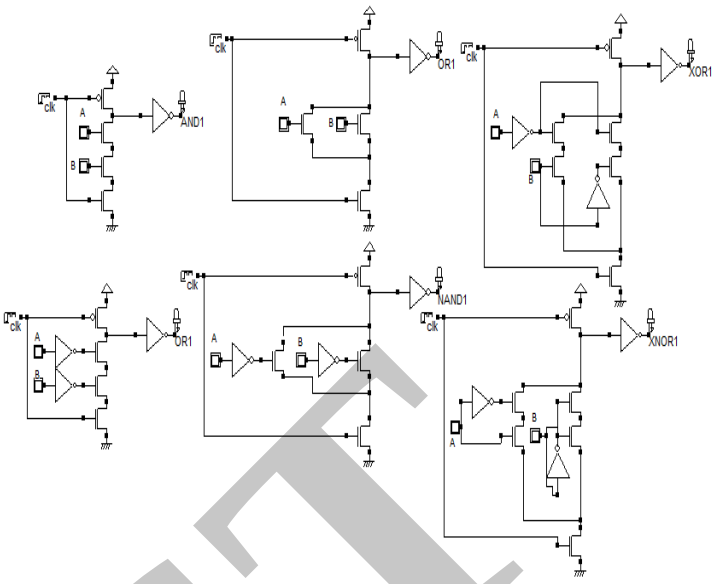


Fig. 2 Primitive Gates using Dynamic Circuit

Self-resetting CMOS logic

III. SELF-RESETTING CMOS DYNAMIC LOGIC

Self-resetting logic is a commonly used piece of circuitry that automatically precharge themselves (i.e., reset themselves) after a prescribed delay. They find applications where a small percentage of gates switch in a cycle, such as memory decoder circuits. It is a form of logic in which the signal being propagated is buffered and used as the precharge or reset signal. By using a buffered form of the input, the input loading is kept almost as low as in normal dynamic logic while local generation of the reset assures that it is properly timed and only occurs when needed [6].

A generic view of a self-reset logic is shown in Fig.3. In the domino case, the clock is used to operate the circuit. In the self-resetting case, the output is fed back to the precharge control input and, after a specified time delay, the pull-up is reactivated. There is an NMOS sub block where the logic function performed by the gate is implemented which is represented as NMOS_LF through which the input data's are loaded. The output of the gate F provides a pulse if the logic function becomes true. This output is buffered and it is connected to PMOS structure to precharge. The delay line is implemented as a series of inverters. The signals that propagate through these circuits are pulses. The width of the pulses must be controlled carefully or else there may be contention between NMOS and PMOS devices, or even worst, oscillations may occur.

One of the advantages of self-resetting logic is that when data present at evaluation does not require dynamic node to discharge, the precharge device is not active hence reduces

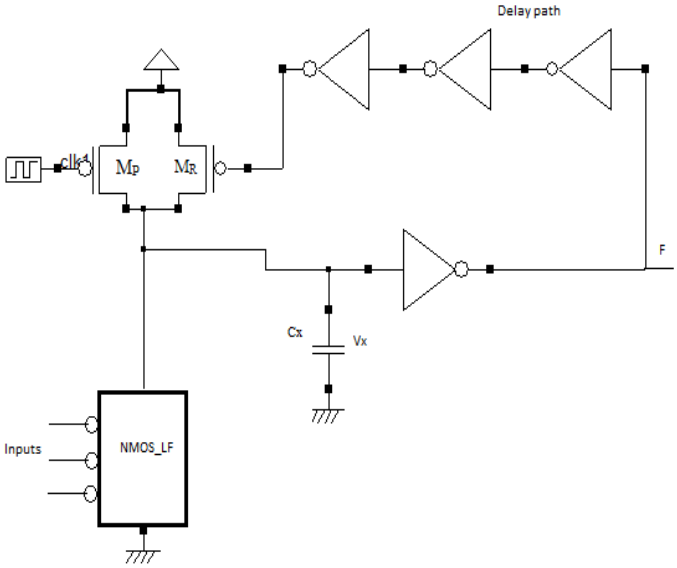
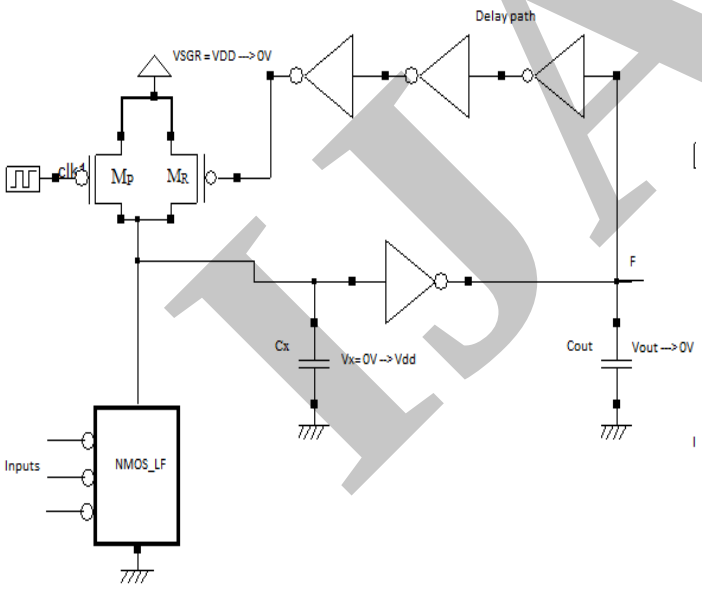
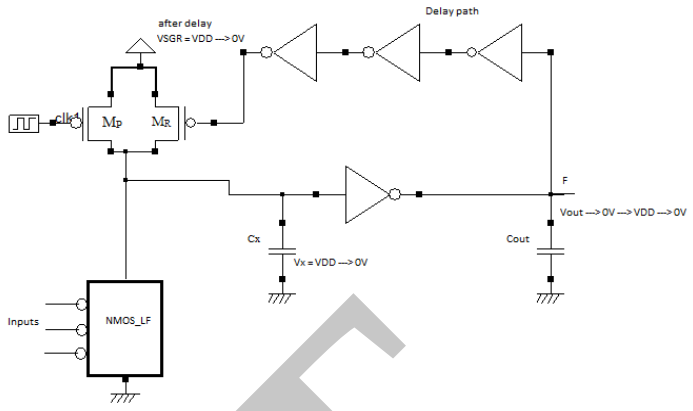


Fig. 3. Self-resetting logic

power [7]. The basic operation of the circuit is shown in Fig. 4. In the circuit M_P,M_R and V_{SGR} represents the precharge pull-up, reset pull-up and gate-source voltage of resetting transistor. During precharge phase clk=0, the transistor M_P turns ON and the pull down network is OFF. Therefore the capacitor is charged to V_{DD}. During evaluation phase clk=1, the transistor M_P turns OFF and the pull down network is ON and evaluates the logic function. Therefore the capacitor is discharged making M_R active which allows I_{DR} to flow and recharge C_X back up to a voltage of V_x=V_{DD}.



a. Precharge



b. Evaluation mode

Fig. 4. Operational modes of self-resetting circuit

IV. SRL PRIMITIVE GATES AND ADDER

This section presents the basic construction and simulation of primitive gates and adders.

A. Primitive gate design

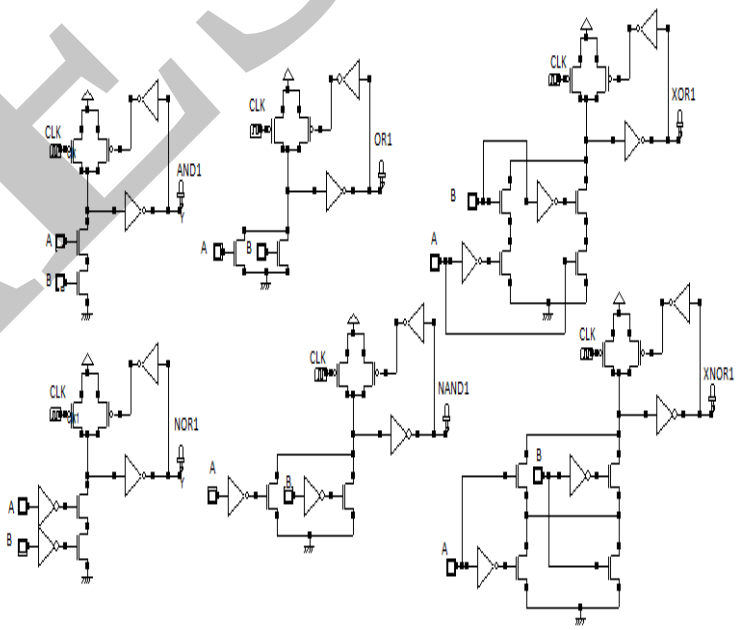


Fig. 5 SRL Primitive Gates

The cells shown in Fig. 5 is a self-resetting implementation of 2-input primitive gates. The logical functions are implemented by the NMOS stack with two input signals A and B. The delay path in this circuit is implemented with single inverter. The mechanism of self-resetting in this circuit is achieved through the PMOS transistors. The implementation of AND/OR can be obtained by placing the NMOS stack in series and parallel

connection, whereas the gates NAND/NOR can be implemented with De Morgan's law, an OR gate with inverted input signals behaves as a NAND gate. Similarly an AND gate with inverted input signals behaves as a NOR gate [8]. However, it is observed that the logic functionality refers to operations on ―pulses" at inputs, and, if no pulses are present at the inputs, the outputs will remain at logic LOW state. The waveforms in Fig. 6 shows the result of spice simulation of primitive gates, implemented in a 0.12-µm CMOS process with VDD = 1.2V. In the waveform the first three waveforms from the top correspond to input signals clk, A and B, followed by the output signals AND1, OR1, NOR1, NAND1, XOR, XNOR1.

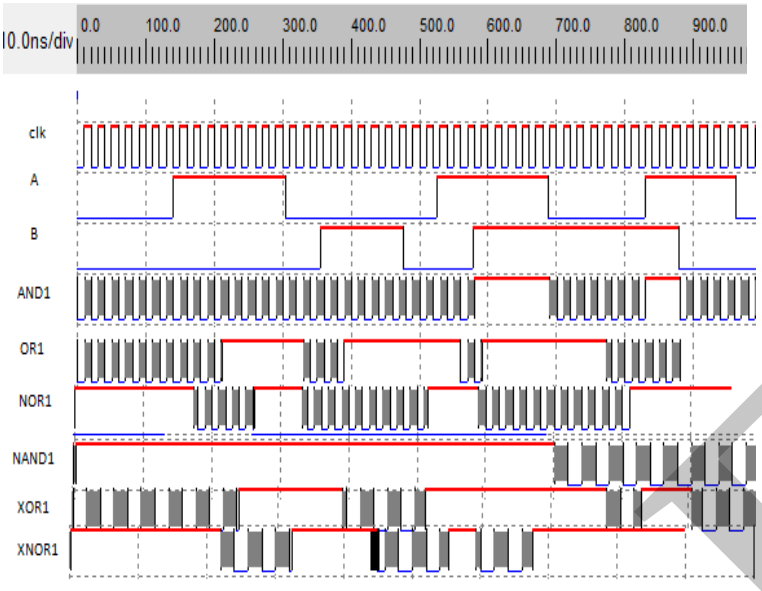


Fig. 6 Simulation of SRL Primitive Gates

B. SRL Full adder design

The SRL full adder circuit is shown in Fig. 7. This adder consists of sum and carry block. The sum block is implemented by SRL XOR and SLR XNOR gates. The carry block is implemented with SRL AND and SLR OR gates. The input to this full adder circuit are A and B, and the outputs are SUM and Cout. Results of SPICE simulation of the adder, implemented in a 0.12µm CMOS process, running at 500MHz data rate, with VDD = 1.2V is shown in Fig. 8.

The sum output can be obtained by

$$X = A \oplus B$$

$$\bar{X} = \overline{A \oplus B}$$

$$SUM = C \oplus X = C\bar{X} + \bar{C}X$$

The carry output is obtained by using the expression
Cout = AB+BC+AC

The simulation cycle for this adder is 500 ns and the input combinations are fed into the system and its performance was

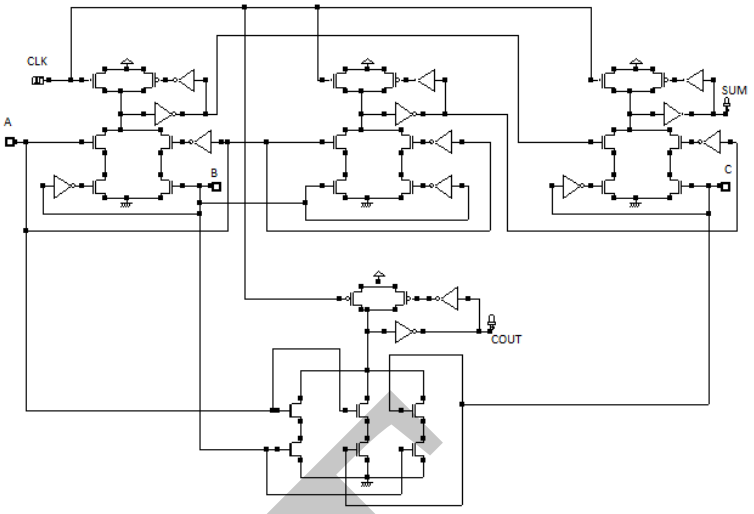


Fig. 7 SRL Full Adder Design

analyzed. It is observed that the adder implemented with dynamic logic has more latency when compared to SRL adder and the power dissipation of SRL adder is less when compared to dynamic logic design.

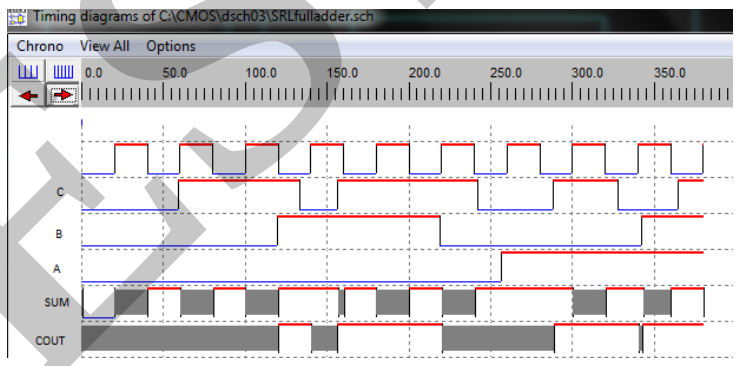


Fig. 8 Simulation of SRL Full Adder Design

C. SRL 4-bit Parallel Adder Design

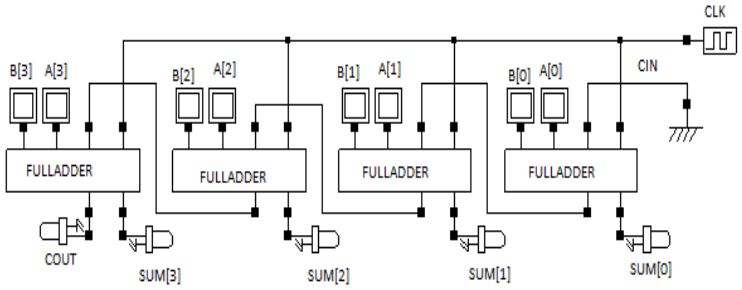


Fig. 9 SRL 4-bit Parallel Adder design

Using the SRL full adder circuit, the SRL 4-bit parallel is implemented as shown in Fig. 9. In this adder circuit, the input to each full-adder will be A_i, B_i and C_i, and the outputs will be SUM_i and $_{Ci+1}$, where _i' varies from 0 to 3. Also, the carry output of the lower order stage is connected to the carry

input of the next higher order stage. In the least significant stage A_0, B_0 and C_0 (which is grounded) are added resulting in SUM[0] and C[1]. This carry C[1] becomes the carry input to the second stage. Similarly the remaining stages are executed. The simulation setup cycle for is adder is 500 ns and the input combinations are fed into the system and its performance was analyzed. Results of SPICE simulation of the adder, implemented in a 0.12µm CMOS process, running at 500MHz data rate, with VDD = 1.2V is shown in Fig. 10.

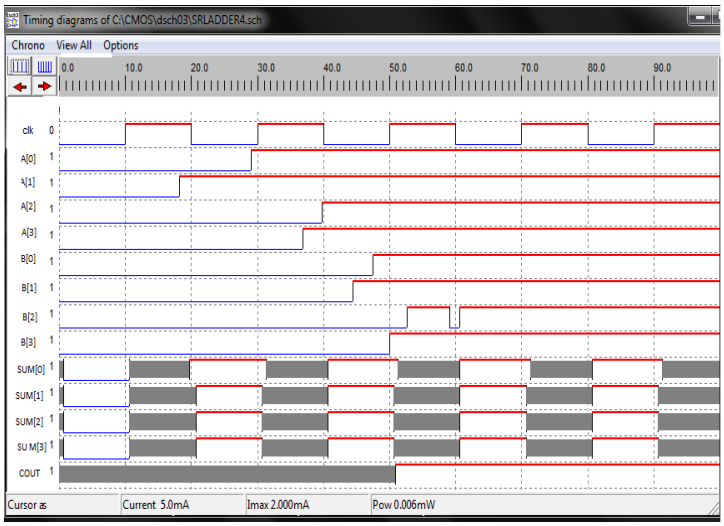


Fig. 11 Simulation of SRL 4-bit Parallel Adder design

D. SRL 4-bit carry look ahead adder

The propagation delay occurred in the parallel adders can be eliminated by carry look ahead adder. This adder is based on the principle of looking at the lower order bits of the augend and addend if a higher order carry is generated. This adder reduces the carry delay by reducing the number of gates through which a carry signal must propagate. This adder consists of three stages: a propagate block/ generate block, a sum generator and carry generator. The generate block can be realized using the expression

$$G_i = A_iB_i \qquad \text{for i=0,1,2,3} \qquad (1)$$

Similarly the propagate block can be realized using the expression

$$P_i = A_i \oplus B_i \quad \text{for i=0,1,2,3} \qquad (2)$$

The carry output of the (i-1)th stage is obtained from

$$C_i(\text{cout}) = G_i + P_iC_{i-1} \quad \text{for i=0,1,2,3} \quad (3)$$

The sum output can be obtained using

$$S_i = A_i \oplus B_iC_{i-1} \quad \text{for i=0,1,2,3} \qquad (4)$$

Fig. 12 shows the implementation of 4-bit carry look ahead adder with the primitive gates explained in the section III is used. Results of SPICE simulation of the adder, implemented in a 0.12µm CMOS process, running at 500MHz data rate, with VDD = 1.2V is shown in Fig. 13.

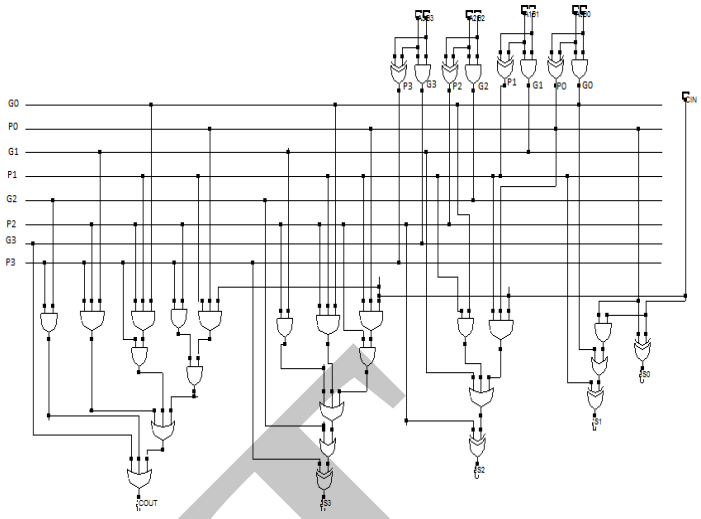


Fig. 12 SRL 4-bit Carry Look Ahead Adder Design

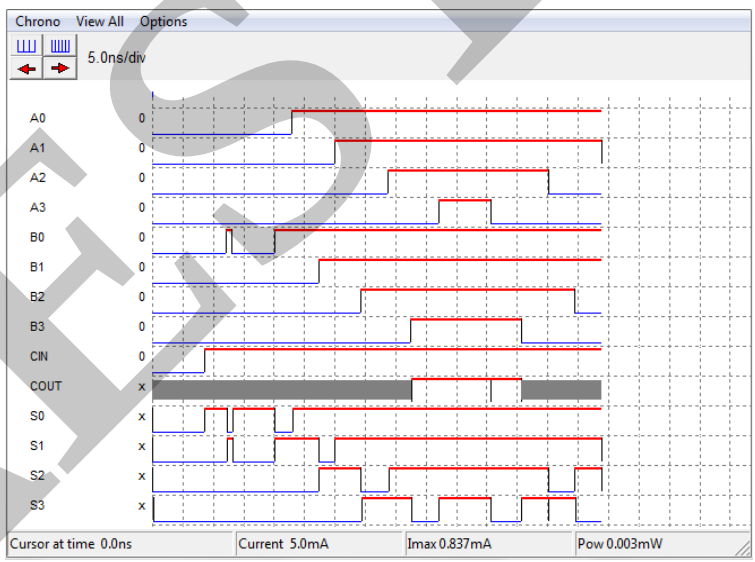


Fig. 13 Simulation of SRL 4-bit Carry Look Ahead Adder Design

V. RESULT

To evaluate performance; primitive gate and adder structures discussed in this paper was designed using 0.12µm CMOS technology. All simulations are carried out at nominal conditions: VDD=1.2 V, I/O supply voltage:2.5 V and room temperature= 27 °C. The device model used in this simulation is empirical level 3, monte-carlo (normal dist. 20%) with the following MOSFET model parameter:

```
* n-MOS Model 3 :
* low leakage
.MODEL N1 NMOS LEVEL=3 VTO=0.40 UO=600.000 TOX= 2.0E-9
+LD =0.000U THETA=0.500 GAMMA=0.400
+PHI=0.200 KAPPA=0.060 VMAX=120.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
```

```
* p-MOS Model 3:
* low leakage
.MODEL P1 PMOS LEVEL=3 VTO=-0.45 UO=200.000 TOX= 2.0E-9
+LD =0.000U THETA=0.300 GAMMA=0.400
+PHI=0.200 KAPPA=0.060 VMAX=110.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
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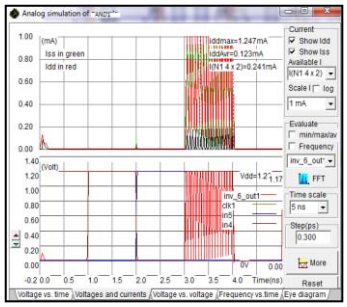
The simulated result for the maximum and average drain current I_{DDMAX} and I_{DDAVG} is shown in Fig. 14.



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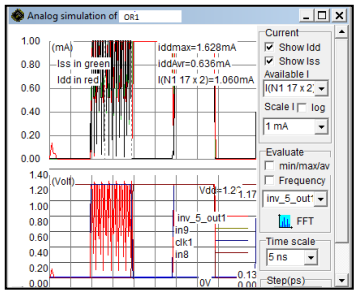

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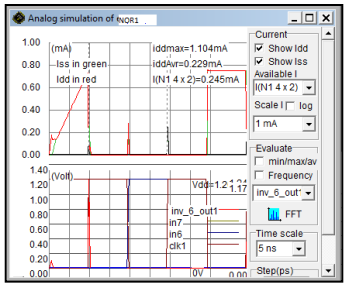

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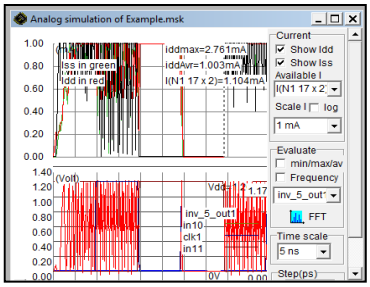

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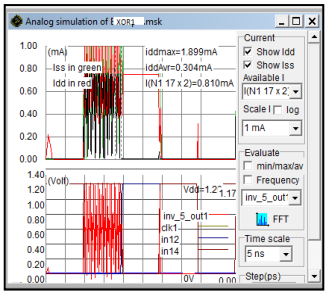

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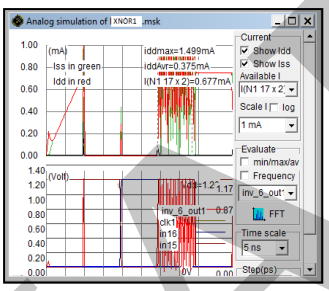

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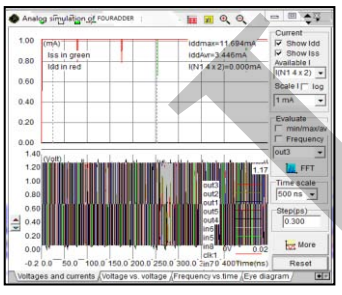

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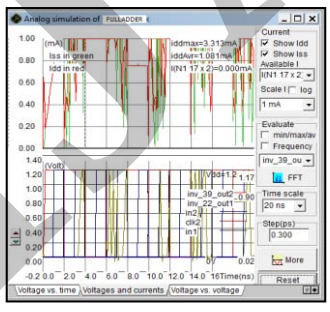

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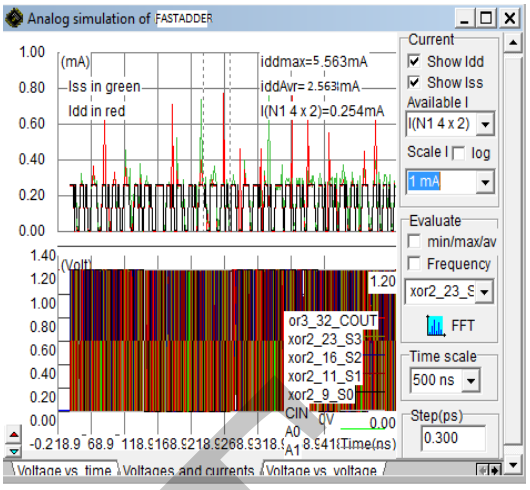
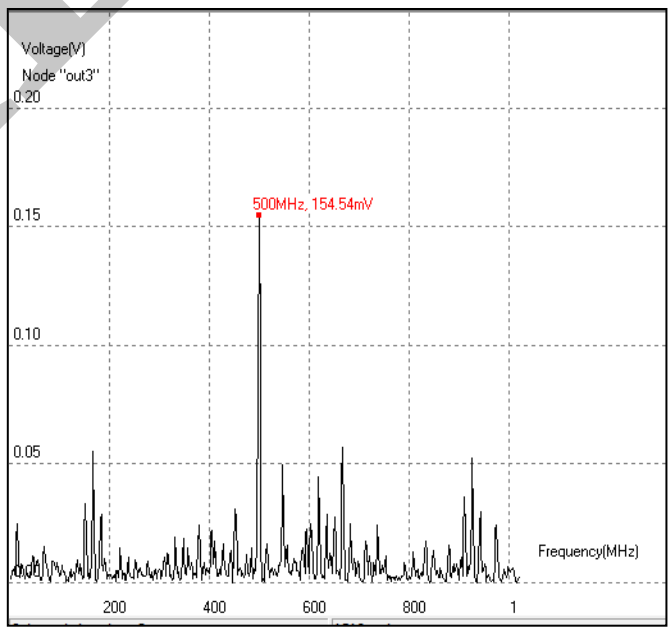


i

Fig 14. Simulated result for the maximum and average drain current I_{DDMAX} and I_{DDAVG} a. AND1 b. OR1 c. NOR1 d. NAND1 e. XOR1 f. XNOR1 g. Full adder h. parallel adder i. carry look ahead

From the simulation it is observed that the maximum drain current for SRL topology is higher than the conventional dynamic circuits. Moreover the leakage current is minimum for SRL logic whereas the leakage current is high for dynamic circuits. The Bessel function is plotted for SRL parallel adder and SRL carry look ahead adder. For clock frequency of 500MHz the maximum power dissipation is 154.54mV and 156.78mV for SRL parallel adder and SRL carry look ahead adder. Fig. 15 shows the Bessel function of parallel and carry look ahead adder.



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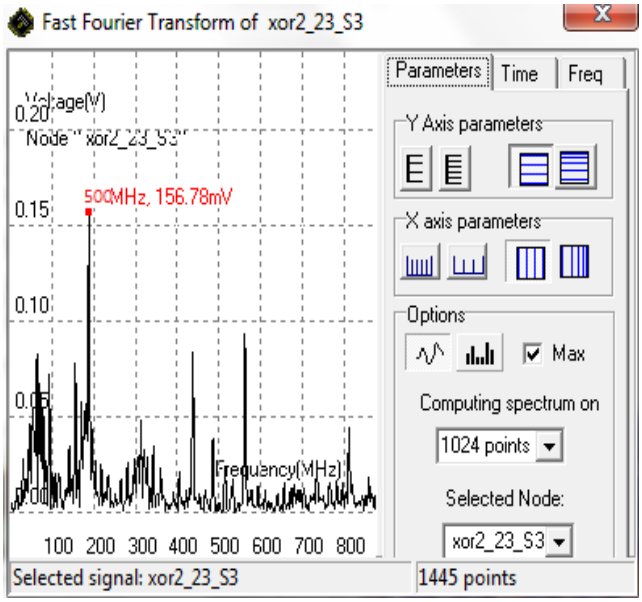

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Fig. 15 Bessel Function a. SRL parallel adder b. SRL carry look ahead adder

VI. SUMMARY

In this section, comparisons of SRL with dynamic logic circuit are discussed. This comparison is done at gate level and performance comparison for specific application like adders is performed. In both cases, it can be shown that SRL can achieve faster, with some leakage power reduction. But the silicon area occupied is slightly more when compare to dynamic logic. In this work, the performances of primitive gates and adder circuit are tested for robustness against area, delay and power dissipation. They are selected for this experiment since they have been commonly used in the industry. Table 1,2,3 and 4 presents the comparison based on parasitic extraction and delay.

Table 1 Parasitic extraction of SRL

Topology	Total Capacitance fF	Total Resistance Ohms	Total Inductance nH (output node)	I_{DDmax} mA	I_{DDAVG} mA
AND1	17.535	1812	0.03	1.247	0.121
OR1	17.164	1834	0.03	1.723	0.654
NOR1	19.867	2273	0.04	1.104	0.229
NAND1	19.3535	2296	0.04	2.761	1.003
XOR1	26.632	2587	0.05	1.899	0.304
XNOR1	26.556	2587	0.05	1.499	0.375
FULL ADDER	96.72	12760	0.29	3.313	1.081
PARALLEL ADDER	330.54	41055	.92	11.69 4	3.446
CARRY LOOK ADHEAD ADDER	135.678	23305	0.42	6.563	2.563

Table 1 Parasitic extraction of Dynamic logic circuit

Topology	Total Capacitance fF	Total Resistance Ohms	Total Inductance nH (output node)	I_{DDmax} mA	I_{DDAVG} mA
AND1	13.789	1222	0.02	0.803	0.002
OR1	13.897	1706	0.03	0.978	0.005
NOR1	14.345	1706	0.03	0.978	0.005
NAND1	13.432	1706	0.03	1.482	0.004
XOR1	19.91	1995	0.04	1.595	0.005
XNOR1	19.90	2098	0.05	1.789	0.059
FULLADDER	92.456	10879	0.05	2.678	0.009
PARALLEL ADDER	320.98	39876	0.06	3.323	1.02
CARRY LOOK ADHEAD ADDER	220	22345	0.42	12.34	3.456

Table3 Power dissipation and area of SRL circuit

Topology	Transistor Count	Rise delay ns(output node)	Fall delay ns(output node)	Pwr Dissipation mW	Area (μm^2)
AND1	8	0.005	0.001	23.12	20.34
OR1	8	0.004	0.001	23.12	20.35
NOR1	12	0.005	0.001	30.45	22.67
NAND1	12	0.015	0.002	30.45	23.56
XOR1	14	0.015	0.002	36.67	35.99
XNOR1	14	0.015	0.002	36.78	36.89
FULLADDER	54	0.050	0.043	45.123	100.9
PARALLEL ADDER	216	0.506	0.498	154.54	1123.89
CARRY LOOK ADHEAD ADDER	205	0.138	0.134	156.78	1120.89

In this comparison the slew rate of the clock signal at each gate in the SRL case is as close as possible to the slew rate of the clock signal at each gate of dynamic circuit. So the power involved in switching at the gate level is fairly comparable. Fig. 16 shows that in SRL the power consumed is about 15% less than the dynamic circuits. All data for area, delay and power dissipation are obtained by microwind tool and simulations performed at the 0.12µm technology with power calculated using Predictive Technology Model (PTM) [10]. The granularity of transistor size is set to the minimum width of 1.02µm and the minimum length of 0.12µm for NMOS and

the minimum width of 1.98 and the minimum length 0.12for PMOS.

Table3 Power dissipation and area of Dynamic logic circuit

Topology	Transistor Count	Rise delay ns(output node)	Fall delay ns(output node)	Pwr Dissipation	Area (μm^2)
AND1	6	0.004	0.002	26.45	18.90
OR1	6	0.002	0.001	26.45	18.92
NOR1	10	0.002	0.001	35.67	20.98
NAND1	10	0.003	0.002	36.67	20.92
XOR1	12	0.003	0.002	47.89	30.45
XNOR1	12	0.003	0.002	47.23	30.54
FULL ADDER	46	0.012	0.01	56.90	90.12
PARALLEL ADDER	184	0.1	0.12	175.65	993.89
CARRY LOOK AHEAD ADDER	202	0.12	0.14	165.76	967.34

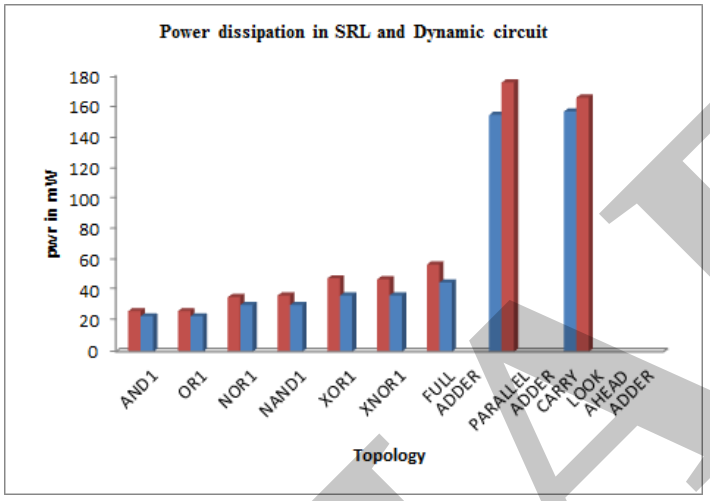


Fig. 16 Power dissipation in SRL and Dynamic circuit

The graph in Fig. 17 shows the distribution of maximum and average drain current for SRL and Dynamic logic circuit. It is observed that for dynamic circuit has the maximum drain current leakage compare to that of SRL.

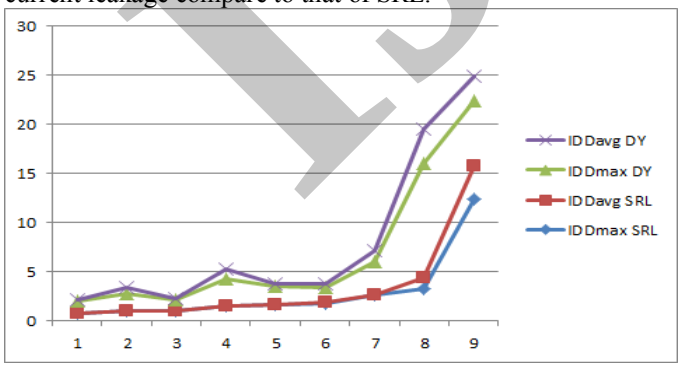
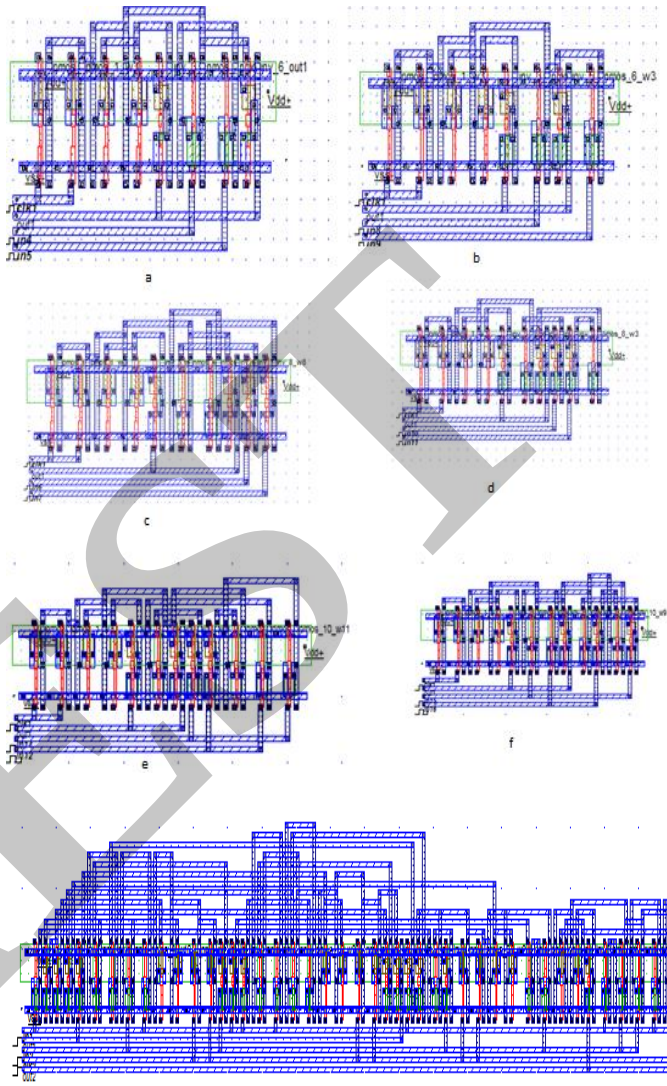
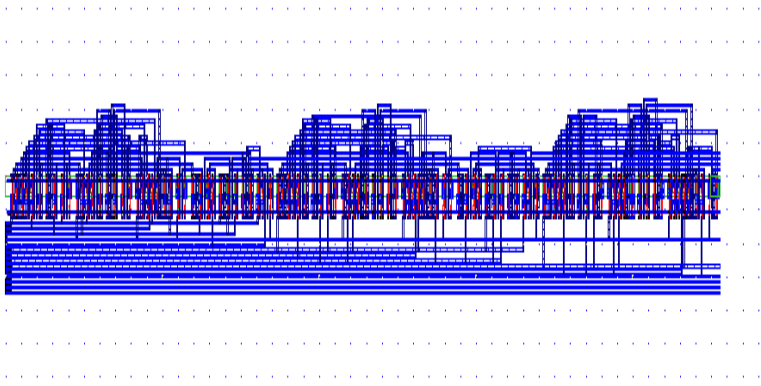


Fig. 17 Current graph of I_{DDMAX} VS I_{DDAVG}.

Finally the layout topology for SRL family id depicted in the Fig. 18





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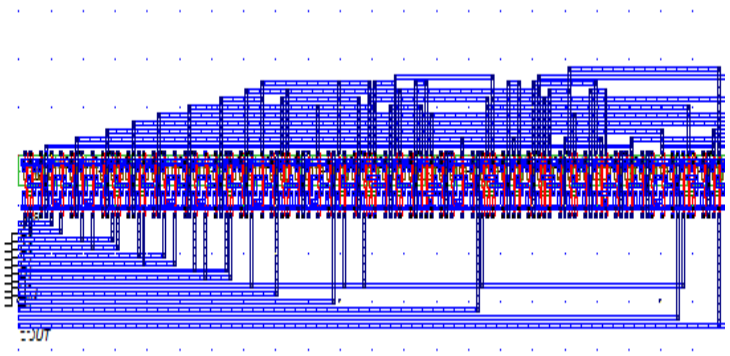

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Fig 18. Layout of SRL a. AND1 b. OR1 c. NOR1 d. NAND1 e. XOR1 f. XNOR1 g. Full adder h. parallel adder i. carry look ahead

VII. CONCLUSION

In this paper, an exhaustive analysis and design methodology for commonly used high-speed primitive gates and adder circuit using self-resetting logic is implemented in 0.12-µm CMOS technologies. The goal was to obtain a family of gates that could simplify the implementation of fast processing circuit which overcomes the restriction due the pulses being elongated and shortened as signal traverse the logic stages. In this paper exhaustive comparison between conventional dynamic logic and SRL were carried in terms of its parasitic value, area and power dissipation. It is observed that the proposed circuits have offered an improved performance in power dissipation, charge leakage and clock skew when compared to dynamic logic with additional burden of silicon area. Hence, it is concluded that the proposed designs will provide a platform for designing high performance and low power digital circuits and high noise immune digital circuits such as, digital signal processors and multipliers.

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